Application No.: 09/638,268   Docket No.: 20421-00074-US

REMARKS

Claims 1-21 are pending in the application. Favorable reconsideration of the case is requested.

Withdrawal of the objection to claims 4 and 13 under 35 U.S.C. § 112 is requested. The claims have been amended to avoid the informalities noted in the Office Action.

Withdrawal of the rejection of claims 1, 3, 4, 12 and 15 under 35 U.S.C. § 103 as being unpatentable over Hellestrand (U.S. Patent 6,263,302) in view of Geer et al. (U.S. Patent 6,212,667) is requested. Additionally, favorable consideration of new claims 17-21 are requested in light of the comments which follow.

The present invention is directed to a method and system for generating test cases which represent bus transactions of a device under test. The bus transactions can be then be applied to a simulator which will emulate a bus protocol for a design under test modeled by hardware description language.

In carrying out the invention, a configuration file is prepared which describes a device under test in terms of bus transactions that it performs. The condensed configuration file is then used to generate all the bus transactions based on various parameter combinations stored in the configuration file. The various bus transactions comprise an output file which is used in a bus simulator to determine if the device under test completely complies with a standardized bus interface.

As set forth in representative claim 1, a design under test configuration file is prepared comprising a specification of bus transactions types and parameters corresponding to a device under test. The configuration file is then processed to generate the test case of bus transactions which are to be verified.

New claims 17-21 further make it clear that the configuration file comprises parameter combinations in a condensed syntax which includes commands and rules to select various

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parameter combinations for inclusion or exclusion from the test case. From the configuration file, all bus transactions are created and stored in the output file of the simulator.

In reviewing the primary reference to Hellestrand, a type of simulator is disclosed wherein a design system 100 provides for simulation of bus transactions. The description 105 of the target digital circuitry includes a bus hardware model 124 for the bus of the target processor. At least some of the operations of the target processor bus may be simulated by running bus hardware model 124 on the hardware simulator. Typically, the user may elect to simulate only some bus transactions that may occur in executing the target processor by running bus hardware model 124 on the hardware simulator (see column 10, lines 24-31). While the ability to simulate the effects of a design on the bus hardware is disclosed in the reference, the reference fails to disclose how test cases can be made to completely test a design under test. In accordance with the foregoing, and the representative claims of the present application, a configuration file is formed of parameter combinations. From the configuration files, bus transactions can be defined by the rules comprising the test case. The bus transactions can then be stored in the output file for a bus simulator.

In reviewing the Hellestrand reference, there doesn't appear to be any description of the kind of file or process for preparing the various test cases to test the bus transactions. While it is understood that the prior art discloses ways for creating bus transactions which can be used to verify a design under test, it is not clear from Hellestrand that there is any process or system which will create a configuration file as set forth in the rejected claims.

Turning now to the Geer et al. reference, a system for generating various test cases to design an integrated circuit is shown. The reference appears to be directed to a process for making certain that the test coverage is adequate for an integrated circuit under test. In the event that the test coverage evaluation is found to be incomplete, an adjustment mechanism is described for creating additional test cases to completely test a design.

In reviewing the reference, it isn't clear where there is any process for creating bus transactions from a configuration file. While there are various tests implemented to check a

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simulated circuit design, nothing appears in the reference to suggest that bus transactions are created from a configuration file of parameters, and used to verify the device under test.

Numerous of Applicants' dependent claims further define the configuration file. For instance, new claims 18-21 require that statements defining transaction types, and command statements which specify parameters associated with each transaction type, be formed in the configuration file. Further, claim 21 makes it clear that the command statements can identify parameters based on a level of significance, and create bus transactions based on the level of significance of the parameter.

Withdrawal of the rejection of claims 2, 13, 14 and 16 under 35 U.S.C. § 103 as being unpatentable over Hellestrand et al., in view of Geer et al., and further in view of Huggins (U.S. Patent 5,956,478) is requested. The addition of a Huggins reference fails to disclose any configuration file which is capable of generating bus transactions. The Huggins device discloses a system for generating test cases for avoiding the generation of an infinitely looping test case. The test case instructions are arranged so that there's only one branch path to a block of instructions, which prevents a branching instruction and a first group of instructions from jumping to a second group of instructions under which a loop can be formed.

Given the fact that the reference does not deal with generating bus transactions, so that a device under test may be fully tested, it is not seen how it can be combined with the foregoing references to render this subject matter obvious. Column 2, lines 35-39, while alluding to the prior art process of generating an automated test case, fails to disclose a generation of a set of transactions from a configuration file where various parameters are stored with rules to define the particular bus transactions of the test.

Withdrawal of the rejections of claims 5-7, under 35 U.S.C. § 103(a) as being unpatentable over Hellestrand et al. in view of Geer et al. further in view of El-Ghoroury et al. (U.S. Patent 5,867,400) is requested. The El-Ghoroury et al. reference describes the architecture and design of an application specific processor. The design originates from various programmable application elements which can be selected to create a specific application. In

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viewing the reference, there isn't any description of any bus transactions which be used to verify a test case.

Withdrawal of the rejection of claim 6 as being unpatentable over Hellestrand et al. (U.S. Patent 6,263,302) in view of Geer et al. and El-Ghouroury et al. further in view of Huggins is requested. In reviewing each of the references, it is not seen where there is any method disclosed which would generate bus transactions from a configuration file of stored parameter values. Accordingly, the combination of references could not yield or disclose these features of Applicants' rejected claims.

Withdrawal of the rejection of claims 8 and 11 under 35 U.S.C. §103(a) as being unpatentable over Hellestrand et al. in view of Geer et al., El-Ghouroury et al. and further in view of Apostol, Jr. et al. (U.S. Patent 6,247,084) and Sheafor et al. (U.S. 6,321,285) is requested. The additional reference also fails to disclose any type of bus transaction which can be created from a configuration file of parameter combinations. Accordingly, the combination fails to suggest these elements of Applicants' claims as well.

In view of the foregoing, favorable reconsideration is believed to be in order. Applicants believe no fee is due with this response. However, if a fee is due, please charge our Deposit Account No. 22-0185, under Order No. 20421-00074-US from which the undersigned is authorized to draw.

Dated: 3/23/04   Respectfully submitted,

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